

### **Amendment to the Specification**

Please replace the paragraph on page 32 with the following paragraph:

Method and system for providing a computer implemented process of performing design for testability analysis and synthesis in an integrated circuit design includes partitioning each logic block in an integrated circuit design based on one or more boundaries of multi-cycle initial setup sequence, excluding one or more partitioned logic blocks with multi-cycle initial setup sequence from valid candidate blocks, selecting a constraint setting set, extracting a subset of constraint settings from the selected constraint setting set, applying the extracted subset of constraint settings to the integrated circuit design, performing design for testability analysis and synthesis on the valid candidate blocks, performing scan cell replacement. The scan cell replacement may include performing class selection from a cell library and a gate-level netlist based on affinity between cells, determining a target characterization, such as timing, power, area, for example, for the scan cell replacement, and replacing one or more cells with a corresponding one or more scan cells having the closest target characteristics.